

NEC 304

STLD

Lecture 28

Timing Analysis

Rajeev Pandey

Department Of ECE

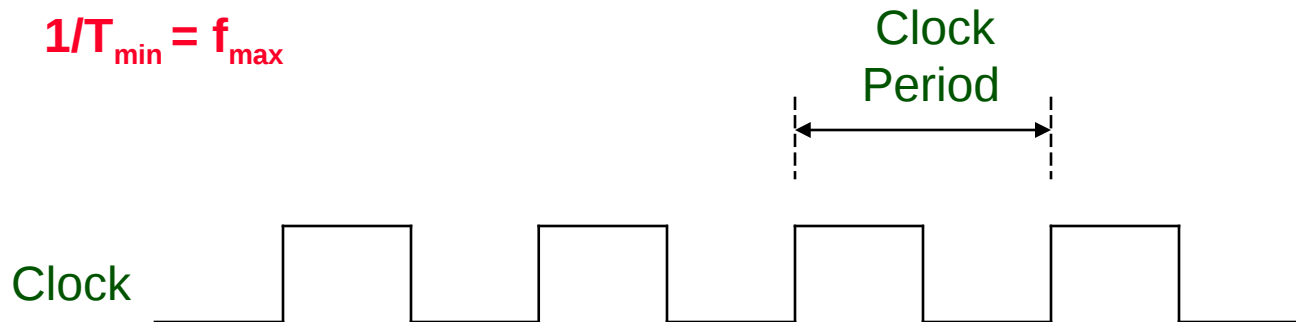
rajeevvce2007@gmail.com

Overview

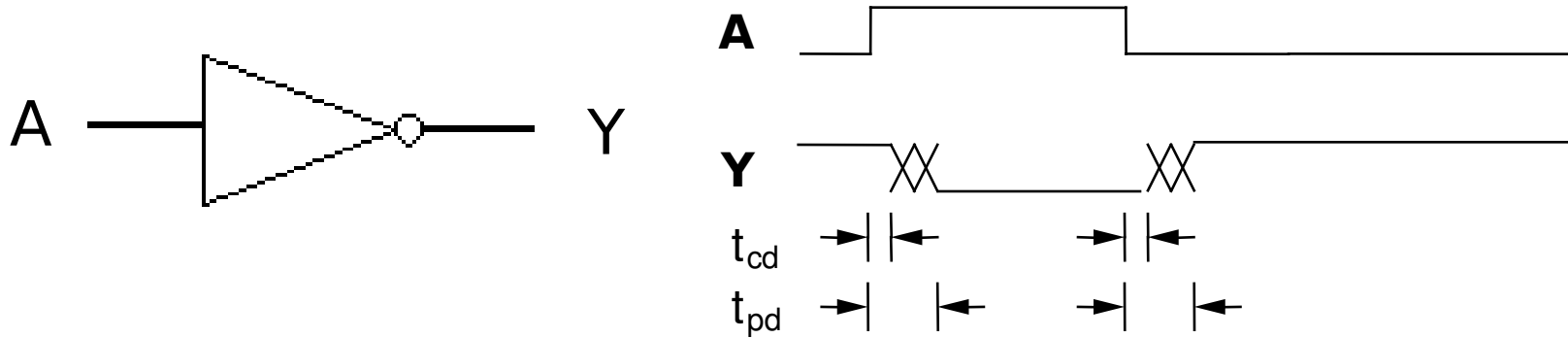
- **Circuits do not respond instantaneously to input changes**
- **Predictable delay in transferring inputs to outputs**
 - **Propagation delay**
- **Sequential circuits require a periodic clock**
- **Goal: analyze clock circuit to determine maximum clock frequency**
 - **Requires analysis of paths from flip-flop outputs to flip-flop inputs**
- **Even after inputs change, output signal of circuit maintains original output for short time**
 - **Contamination delay**

Sequential Circuits

- Sequential circuits can contain both combinational logic and edge-triggered flip flops
- A **clock** signal determines when data is stored in flip flops
- **Goal: How fast can the circuit operate?**
 - Minimum clock period: T_{\min}
 - Maximum clock frequency: f_{\max}
- Maximum clock frequency is the inverse of the minimum clock period
 - $1/T_{\min} = f_{\max}$

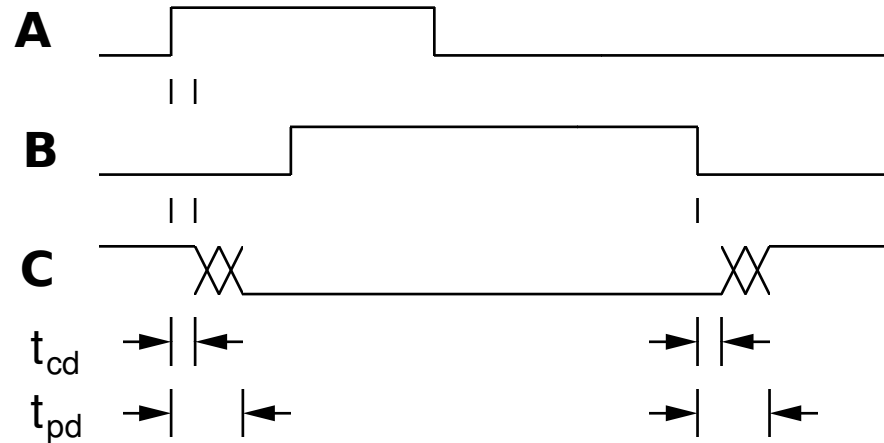
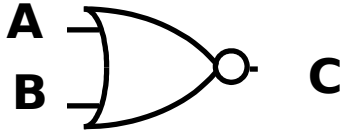


Combinational Logic Timing: Inverter



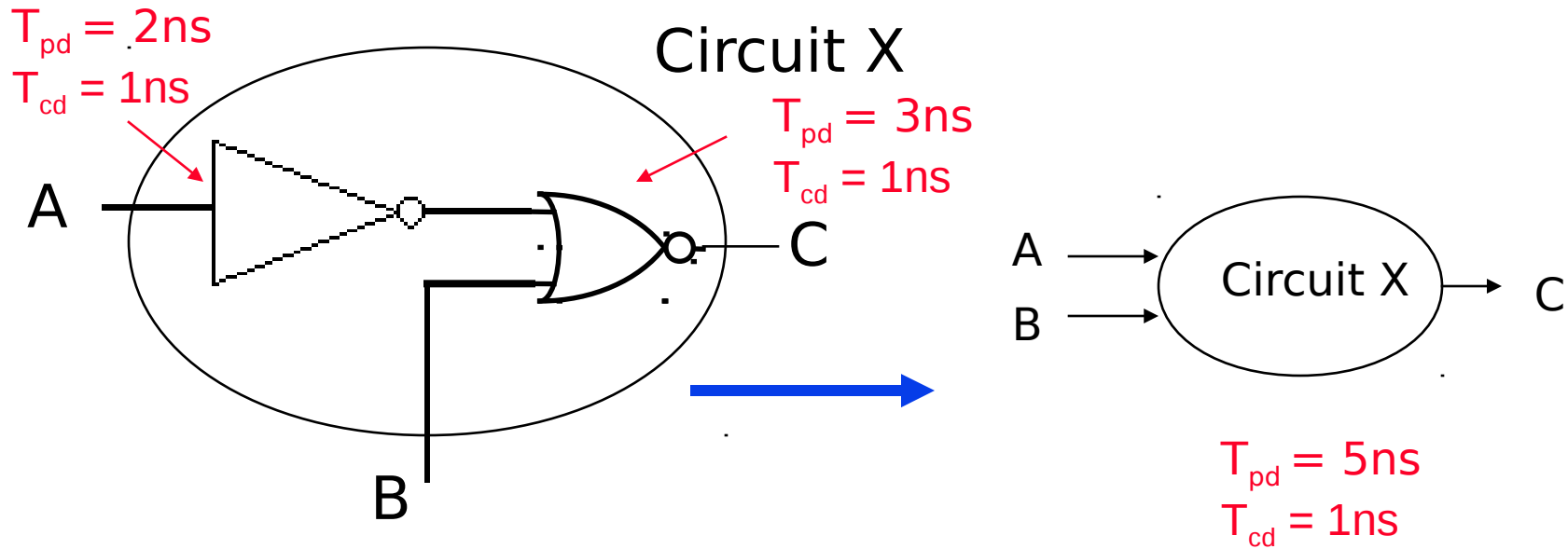
- **Combinational logic is made from electronic circuits**
 - An input change takes time to **propagate** to the output
- **The output remains unchanged for a time period equal to the **contamination delay**, t_{cd}**
- **The new output value is guaranteed to valid after a time period equal to the **propagation delay**, t_{pd}**

Combinational Logic Timing: XNOR Gate



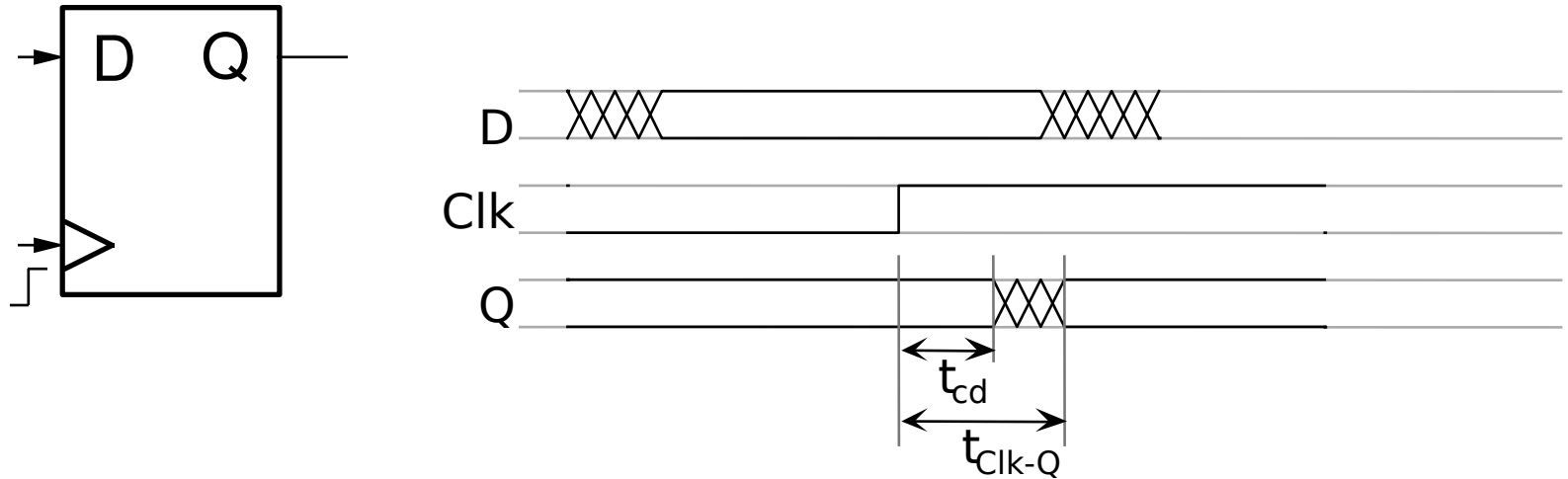
- The output is guaranteed to be stable with **old** value **until** the contamination delay
 - *Unknown values shown in waveforms as Xs*
- The output is guaranteed to be stable with the **new** value **after** the propagation delay

Combinational Logic Timing: complex circuits



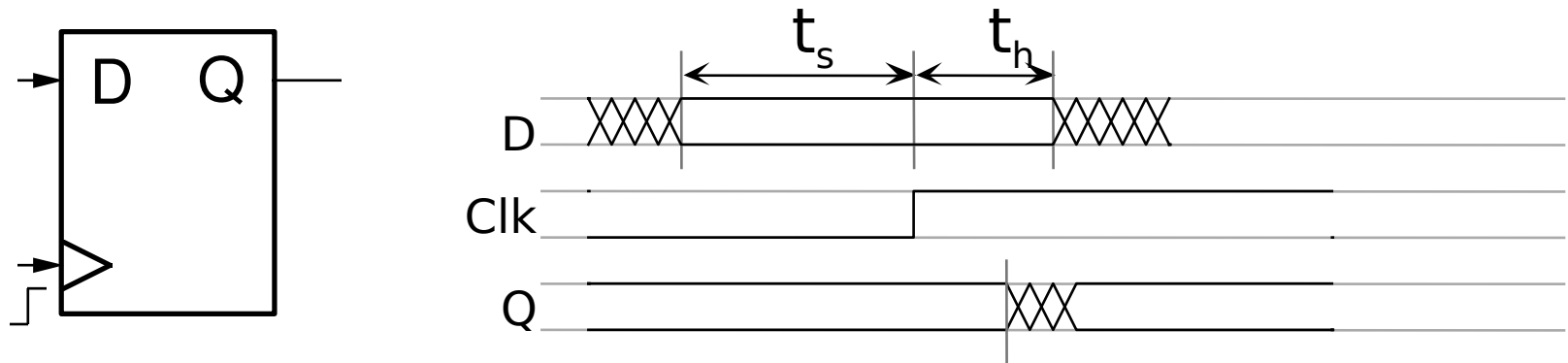
- **Propagation delays are additive**
 - Locate the **longest** combination of t_{pd}
- **Contamination delays may not be additive**
 - Locate the **shortest** path of t_{cd}
- **Find propagation and contamination delay of new, combined circuit**

Clocked Device: Contamination and Propagation Delay



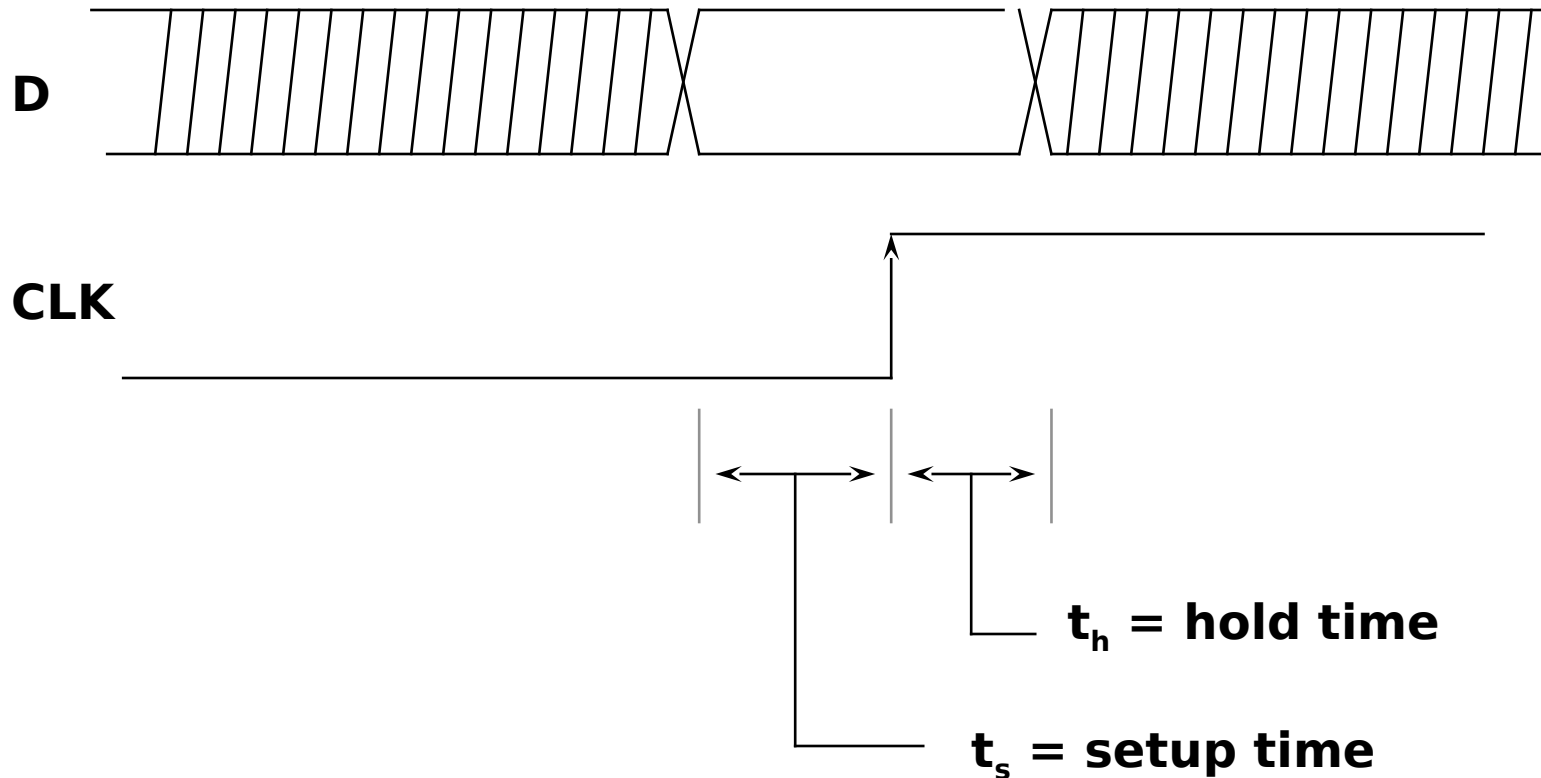
- Timing parameters for **clocked** devices are specified in relation to the **clock input** (rising edge)
- Output unchanged for a time period equal to the **contamination delay**, t_{cd} after the rising clock edge
- New output guaranteed valid after time equal to the **propagation delay**, t_{clk-Q}

Clocked Devices: Setup and Hold Times



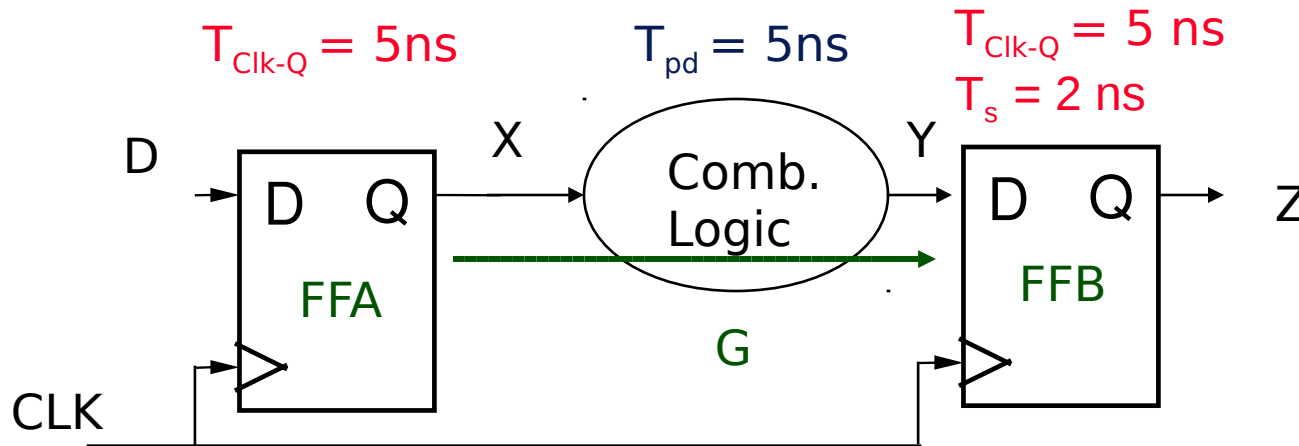
- Timing parameters for **clocked** devices are specified in relation to the **clock input** (rising edge)
- D input **must** be valid at least t_s (**setup time**) before the rising clock edge
- D input **must** be held steady t_h (**hold time**) after rising clock edge
- Setup and hold are input restrictions
 - Failure to meet restrictions causes circuit to operate

Edge-Triggered Flip Flop Timing



- The logic driving the flip flop must ensure that setup and hold are met
- Timing values (t_{cd} t_{pd} $t_{\text{CLK-Q}}$ t_s t_h)

Analyzing Sequential Circuits



° What is the minimum time between rising clock edges?

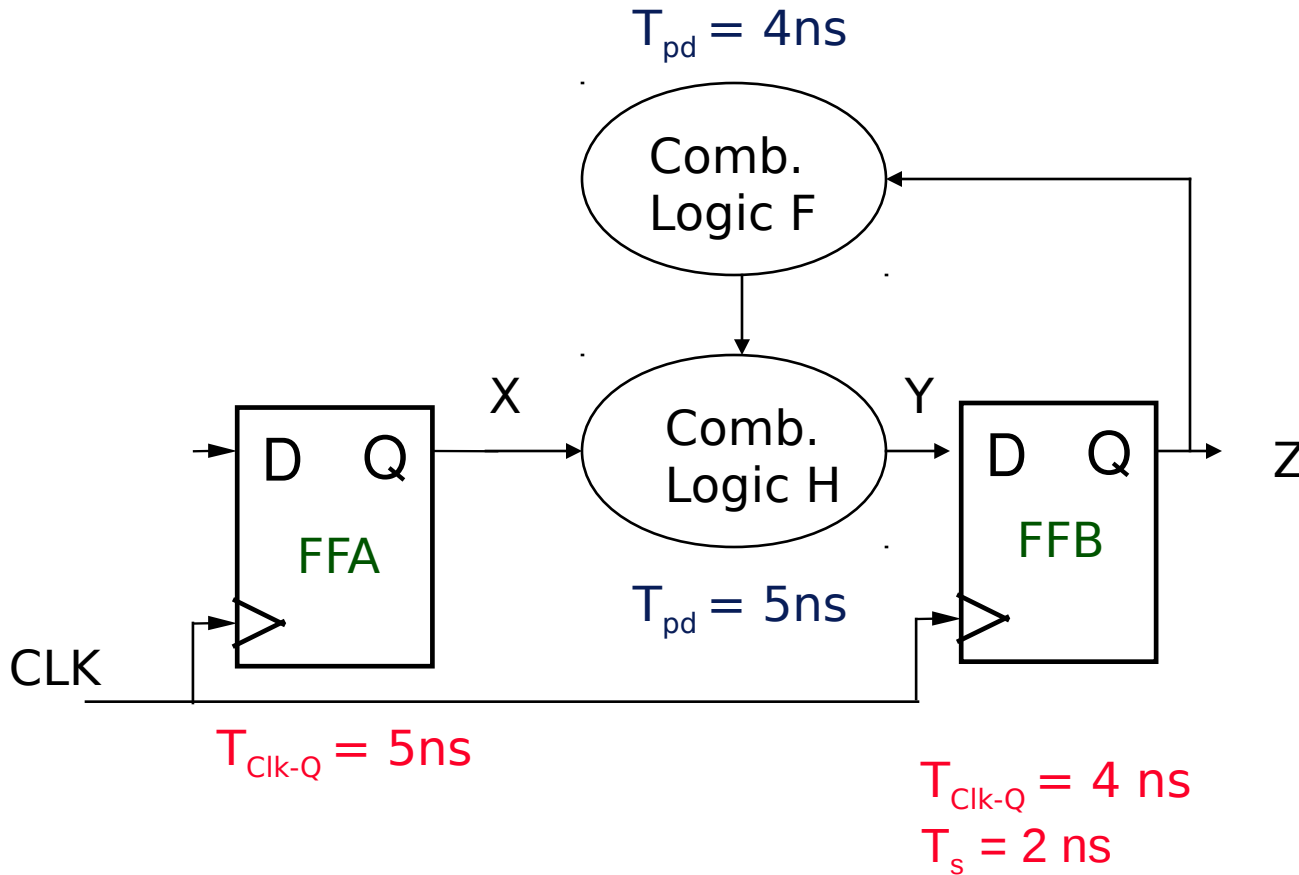
- $T_{\min} = T_{\text{CLK-Q}}(\text{FFA}) + T_{\text{pd}}(\text{G}) + T_s(\text{FFB})$

° Trace propagation delays from FFA to FFB

° Draw the waveforms!

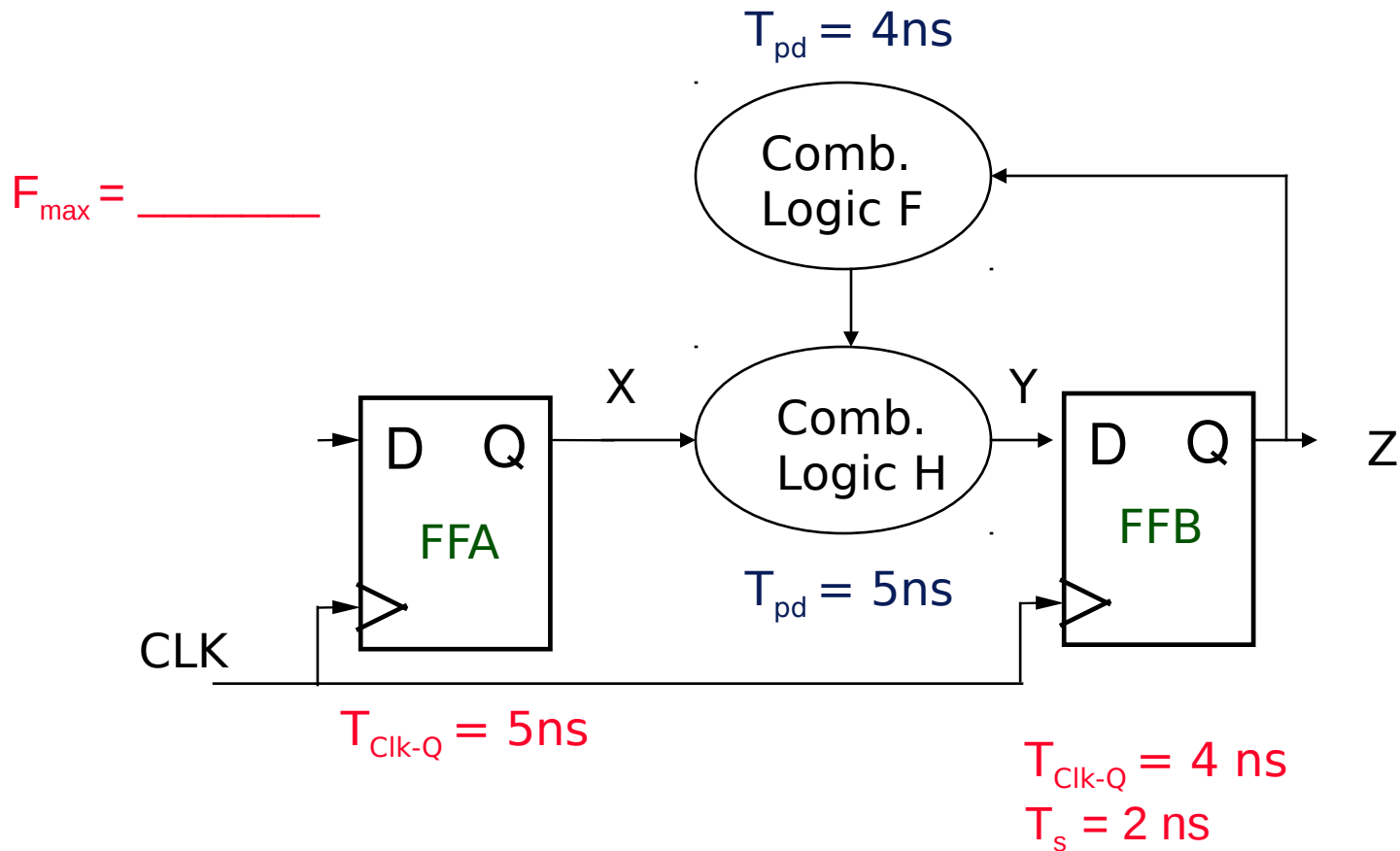
$F_{\max} = \underline{\hspace{2cm}}$

Analyzing Sequential Circuits



- What is the minimum clock period (T_{\min}) of this circuit? **Hint: evaluate all FF to FF paths**
- Maximum clock frequency is $1/T_{\min}$

Analyzing Sequential Circuits



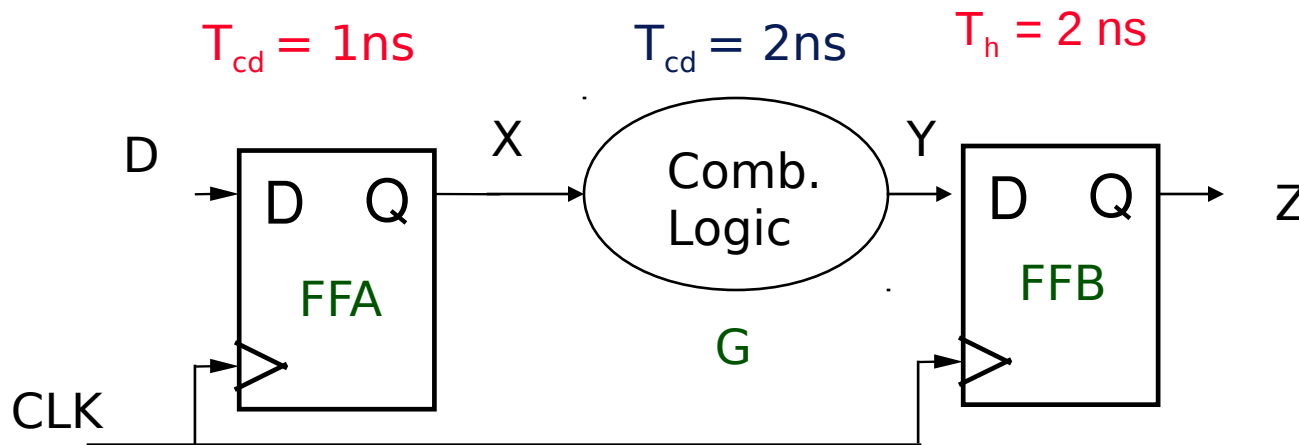
° Path FFA to FFB

- $T_{\text{clk-Q}}(\text{FFA}) + T_{\text{pd}}(\text{H}) + T_s(\text{FFB}) = 5\text{ns} + 5\text{ns} + 2\text{ns} = 12\text{ns}$

° Path FFB to FFB

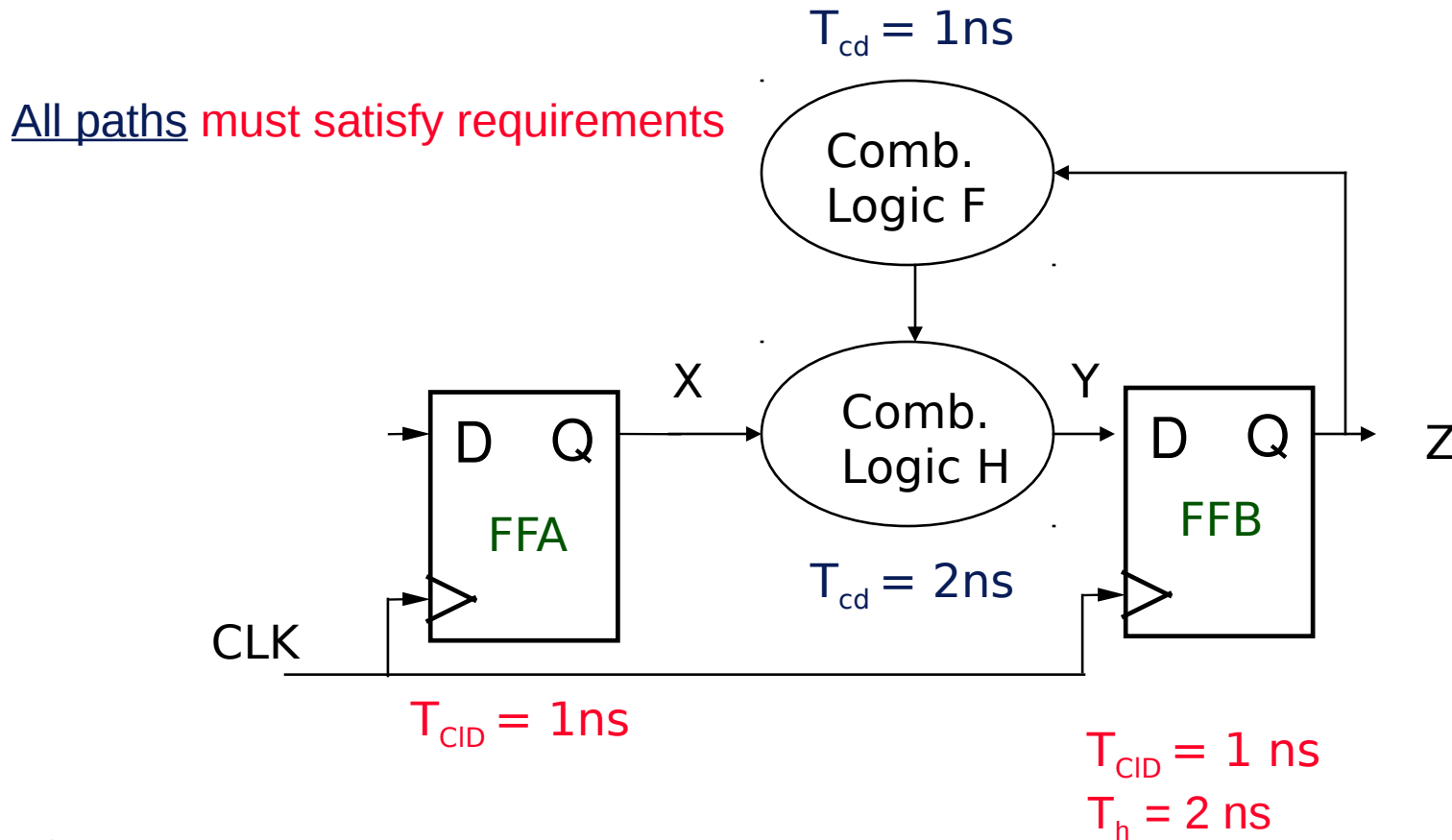
- $T_{\text{clk-Q}}(\text{FFB}) + T_{\text{pd}}(\text{F}) + T_{\text{pd}}(\text{H}) + T_s(\text{FFB}) = 4\text{ns} + 4\text{ns} + 5\text{ns} + 2\text{ns}$

Analyzing Sequential Circuits: Hold Time Violation



- ° One more issue: make sure Y remains stable for hold time (T_h) after rising clock edge
- ° Remember: contamination delay ensures signal doesn't change
- ° How long before first change arrives at Y?
 - $T_{cd}(\text{FFA}) + T_{cd}(\text{G}) \geq T_h$
 - $1\text{ns} + 2\text{ns} > 2\text{ns}$

Analyzing Sequential Circuits: Hold Time Violations



◦ Path FFA to FFB

- $T_{CD}(\text{FFA}) + T_{CD}(\text{H}) > T_h(\text{FFB}) = 1\text{ns} + 2\text{ns} > 2\text{ns}$

◦ Path FFB to FFB

- $T_{CD}(\text{FFB}) + T_{CD}(\text{F}) + T_{CD}(\text{H}) > T_h(\text{FFB}) = 1\text{ns} + 1\text{ns} + 2\text{ns} > 2\text{ns}$

Summary

- Maximum clock frequency is a fundamental parameter in sequential computer systems
- Possible to determine clock frequency from propagation delays and setup time
- The longest path **determines** the clock frequency
- All flip-flop to flip-flop paths must be checked
- Hold times are satisfied by examining contamination delays
- The **shortest** contamination delay path determines if hold times are met
- Check handout for more details and examples.